EGC442
Class Notes
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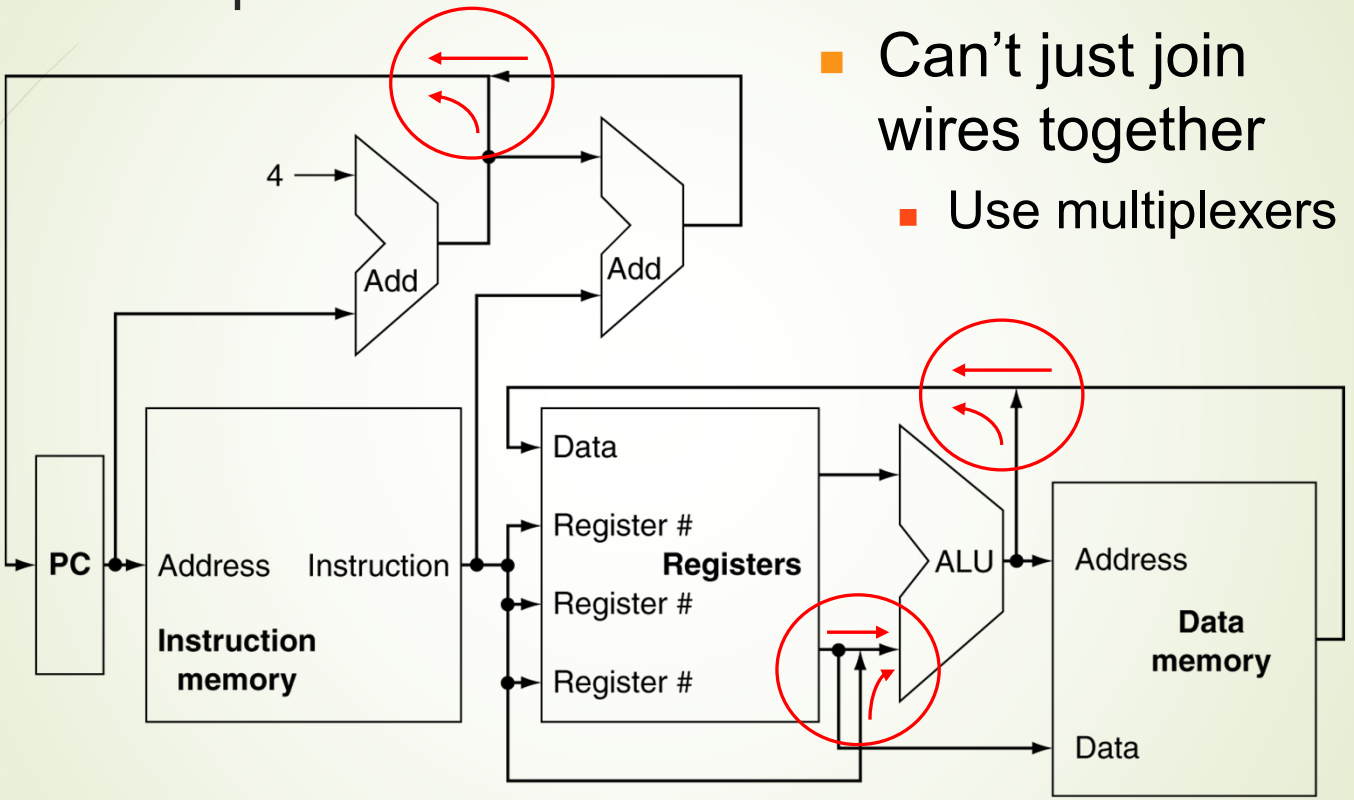
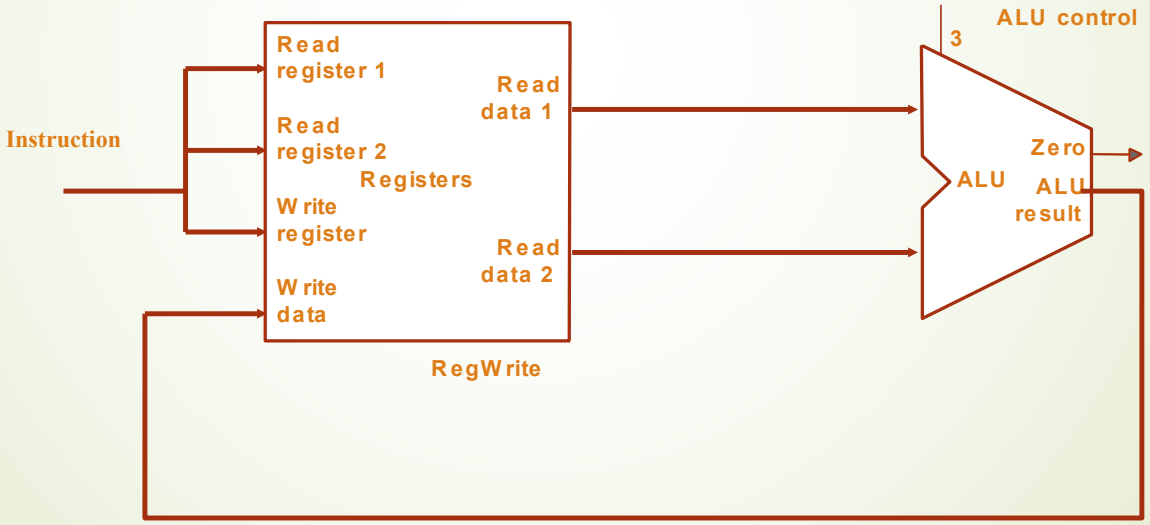
Multiplexers



- Can't just join wires together
  - Use multiplexers

R-Format Instructions

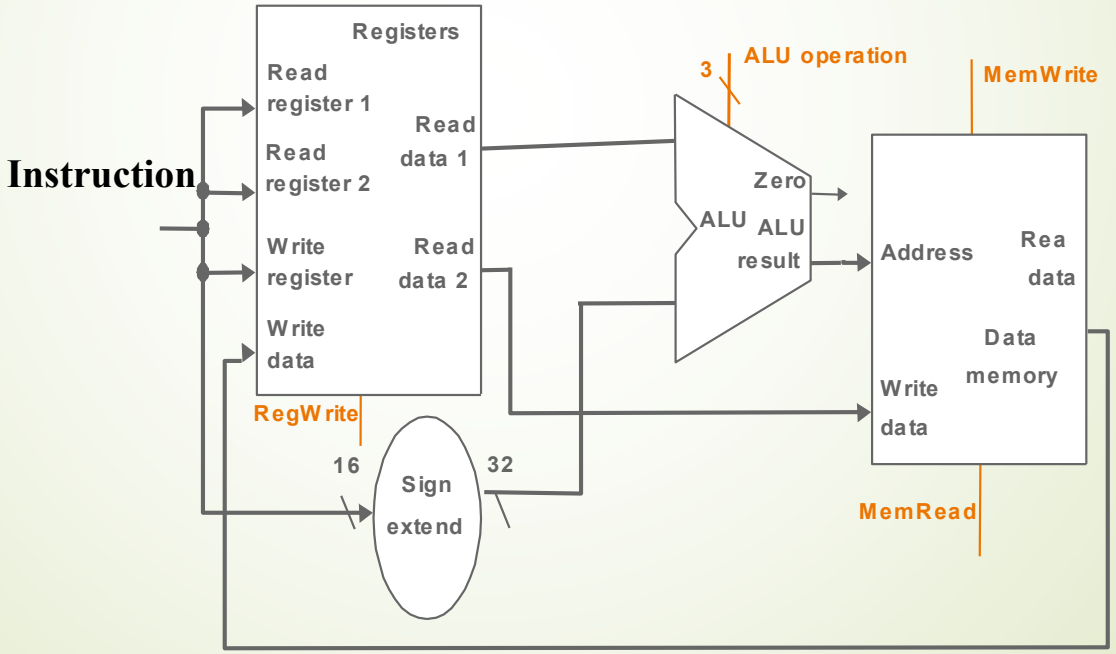
- Read two register operands
- Perform arithmetic/logical operation
- Write register result



Datapath for *lw* and *sw* Insturctions

lw $t1, offset_value($t2) or sw $t1, offset_value ($t2)

- Compute memory address
- Sign extend 16 bit to 32 bit



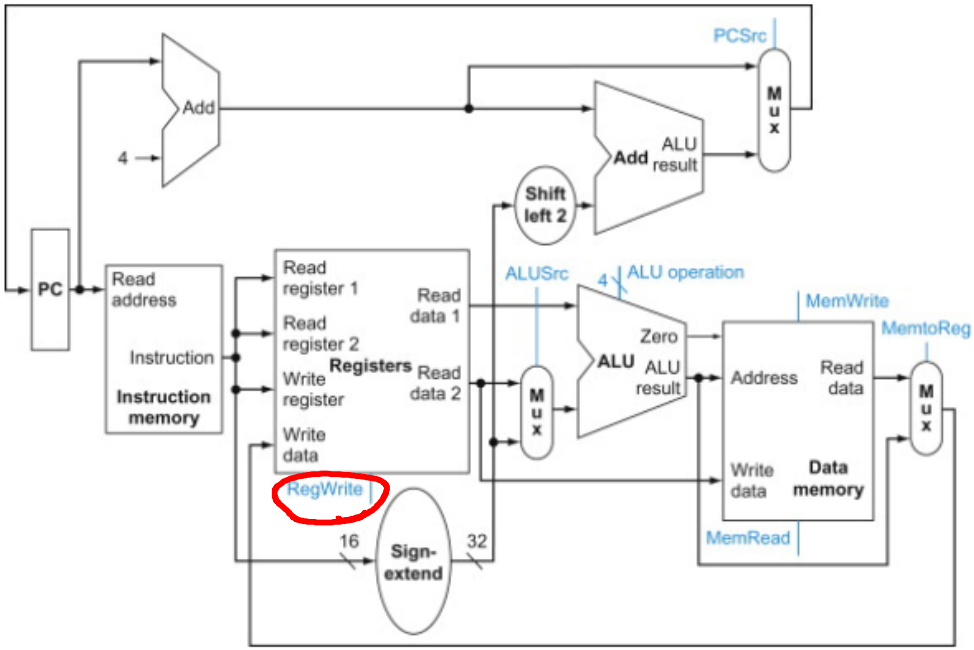
Consider the MIPS datapath of Figure 5.3.5. Find the error in each of the following statements.

1) An R-type instruction like add uses three datapath units: the register file, the ALU, and the data memory.

2) In addition to the register file and ALU, a load or store instruction also involves the sign extension, data memory, and shift left units.

3) The branch datapath uses the sign extension, shift by 2, and data memory units.

4) The mux at the upper right either passes PC +4 (the normal case), or passes a target address from the instruction (for jumps or branches).



Consider the figure above showing the datapath and control unit in Figure 5.4.5 (labeled as "Control"), and table further above listing control unit output signals.

The control unit sends _____ bits to the ALU control.

0

1

2

The control unit enables a write to the register file using the _____ signal.

RegDst

MemWrite

RegWrite

When MemToReg is 0, the data appearing at the register file's data input comes from the _____.

ALU's output

data memory's output

register file's output

The ALU's top input always comes from the Read data 1 output of the register file. The ALU's bottom input can come from two possible places: The Read data 2 output of the register file, or the instruction's lower 16 bits, sign extended to 32 bits. Which control unit output select among those two places?

ALUOp

ALUSrc

Zero

The control unit's Branch output will be 1 for a branch equal instruction. However, the branch's target address is only loaded into the PC if the ALU's Zero output is _____. Otherwise, PC is loaded with PC + 4.

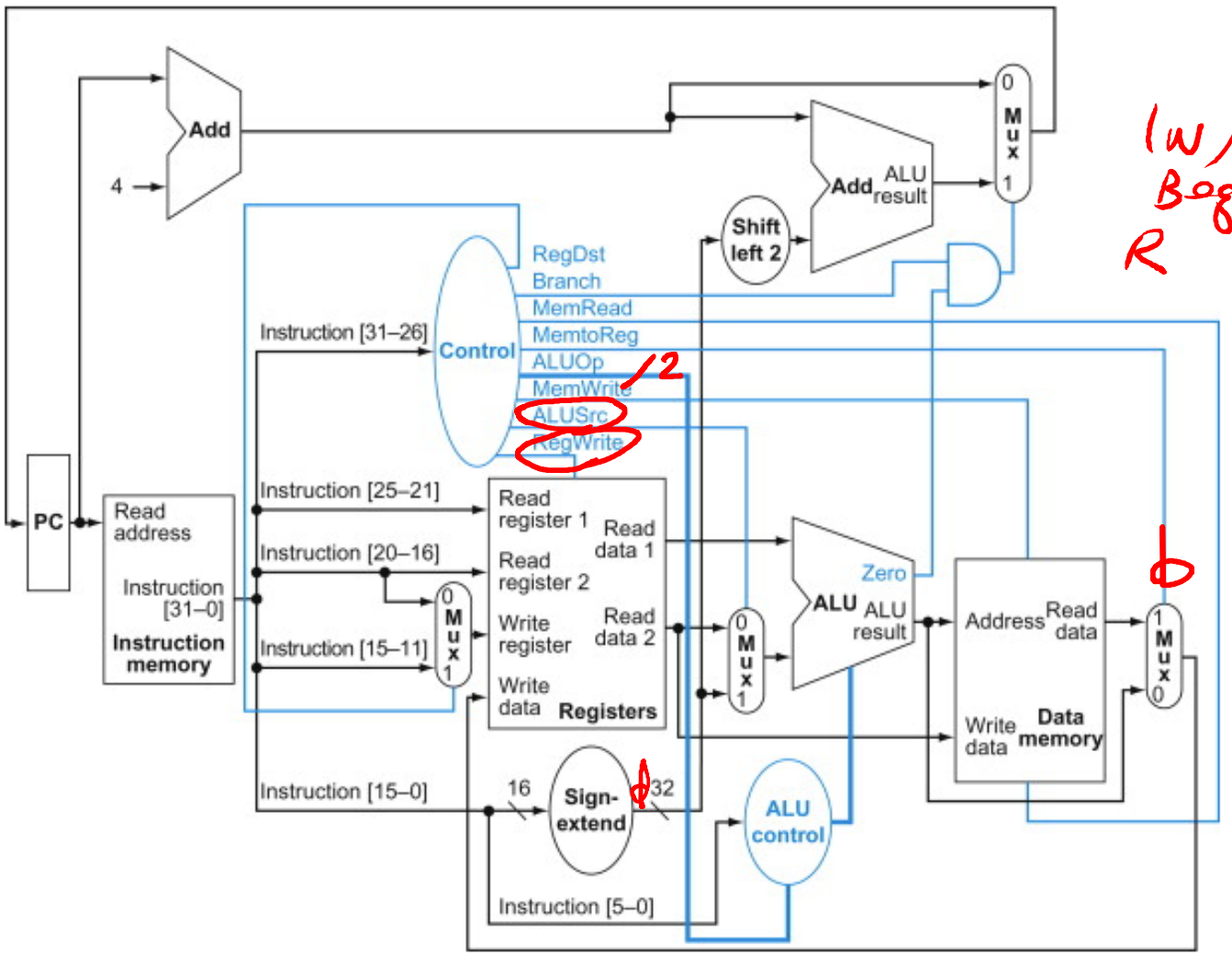
0

1

(actually, Zero is not involved)

rs = rt → rs - rt = 0

Z = 1


Add
4
Add
ALU result
Shift left 2
0
M
u
x
1
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Control
Instruction [31–26]
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign-extend
32
ALU
Zero
ALU result
ALU control
Address
Read data
Write data
Data memory
lw/sw
Beq
R
00
01
10
2
b
4

Consider the above Figure 5.4.8 illustrating the datapath in action for a branch equal instruction.

10) The value for the ALUSrc control signal is ____.
0
1

11) The value for the ALUOp control signal is ____.
00
01

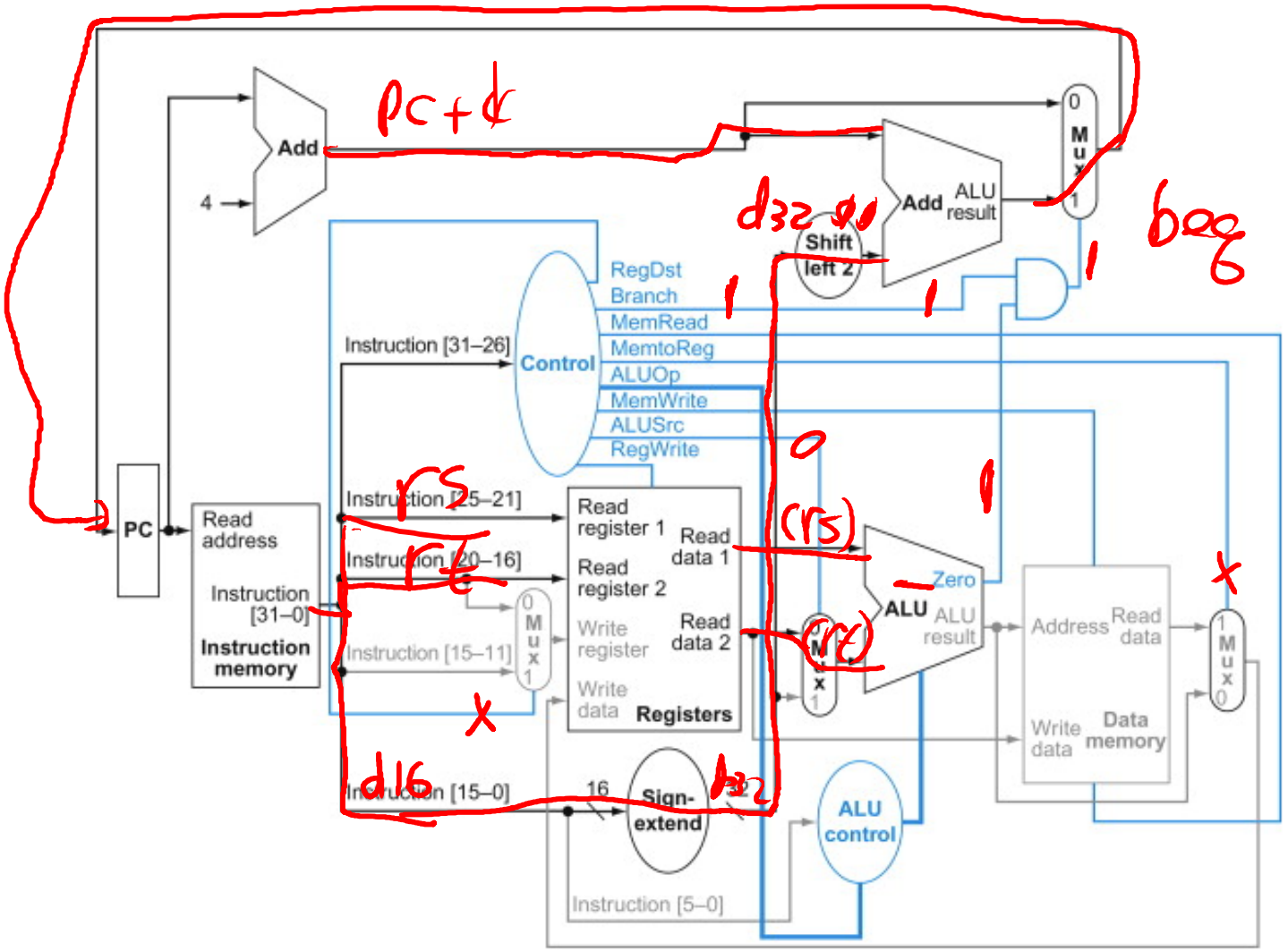
12) Assume the current instruction is beq $t1, $t2, offset, and $t1 is 90 while $t2 is 85. The value for the Branch control signal is ____.
0
1

13) Assume the current instruction is beq $t1, $t2, offset, and $t1 is 90 while $t2 is 85. The value for the Zero control signal is ____.
0
1

14) Assume the current instruction is beq $t1, $t2, offset, and $t1 is 90 while $t2 is 85. How will the PC be updated next?
PC + 4
Target address

115) The datapath shown requires four clock cycles to execute a branch instruction.
True
False

16) During a branch on equal instruction, two registers are read, those registers' values are subtracted. If the result is 0, Zero becomes 1, causing a new target address to pass through the mux on the upper right and be waiting to enter the PC on the next rising clock edge.
True
False


Add
4
Add
ALU result
Shift left 2
M u x
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
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Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign-extend
ALU
Zero
ALU result
ALU control
Address
Read data
Write data
Data memory

17)Highlight the active data path for: *add* *$4, $5, $6*

Annotate the different segments of highlighted datapath with what they carry Assume the instruction is at memory location 0X1000, ($4) = 0X9 , and ($5) = 0X6000, and ($6) = 0X2040

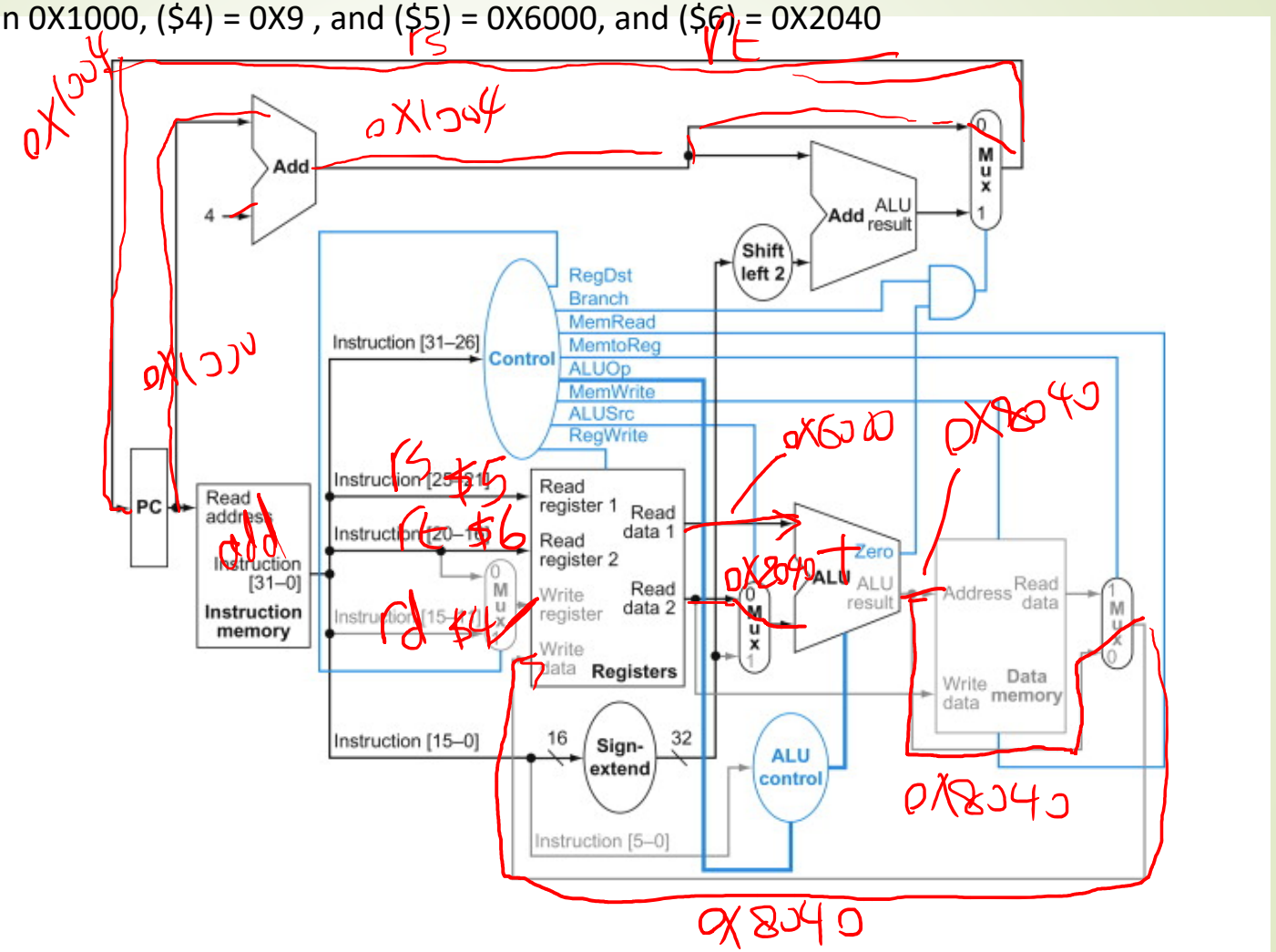
After execution:

$4 = 0X8040

$5= 0X6000

$6= 0X2040

PC= 0X1004



17)Highlight the active data path for: *lw $4, ($5)0x48*

Annotate the different segments of highlighted datapath with what they carry Assume the instruction is at memory location 0X1000, ($4) = 0X9 , and ($5) = 0X6000, and ($6) = 0X2040 Mem[0x6048] = 0x248E

After execution:

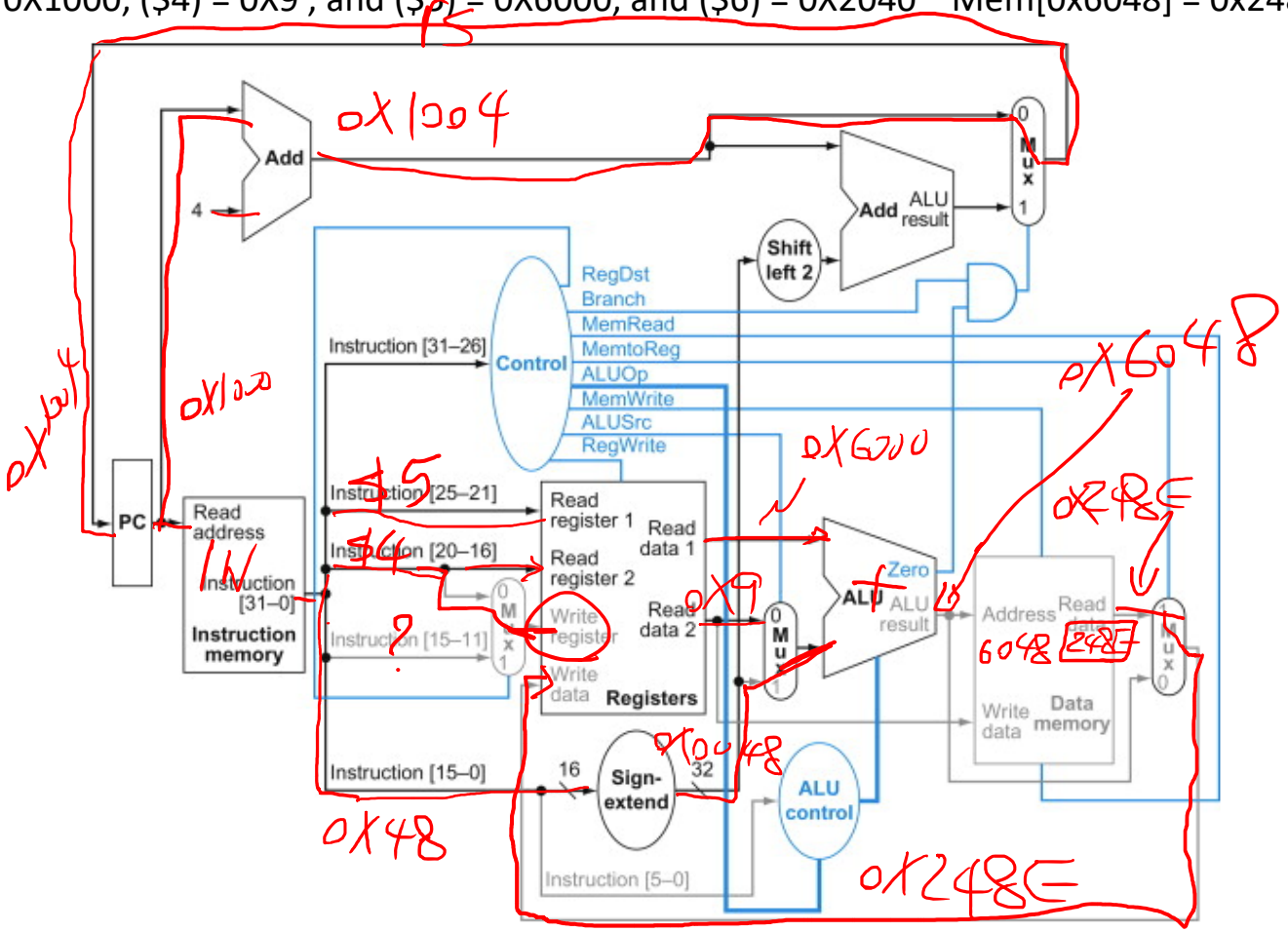
$4 = 0X248E

$5= 0X6000

$6= 0X2040

PC=0X1004

M[0X6048]=0X248E



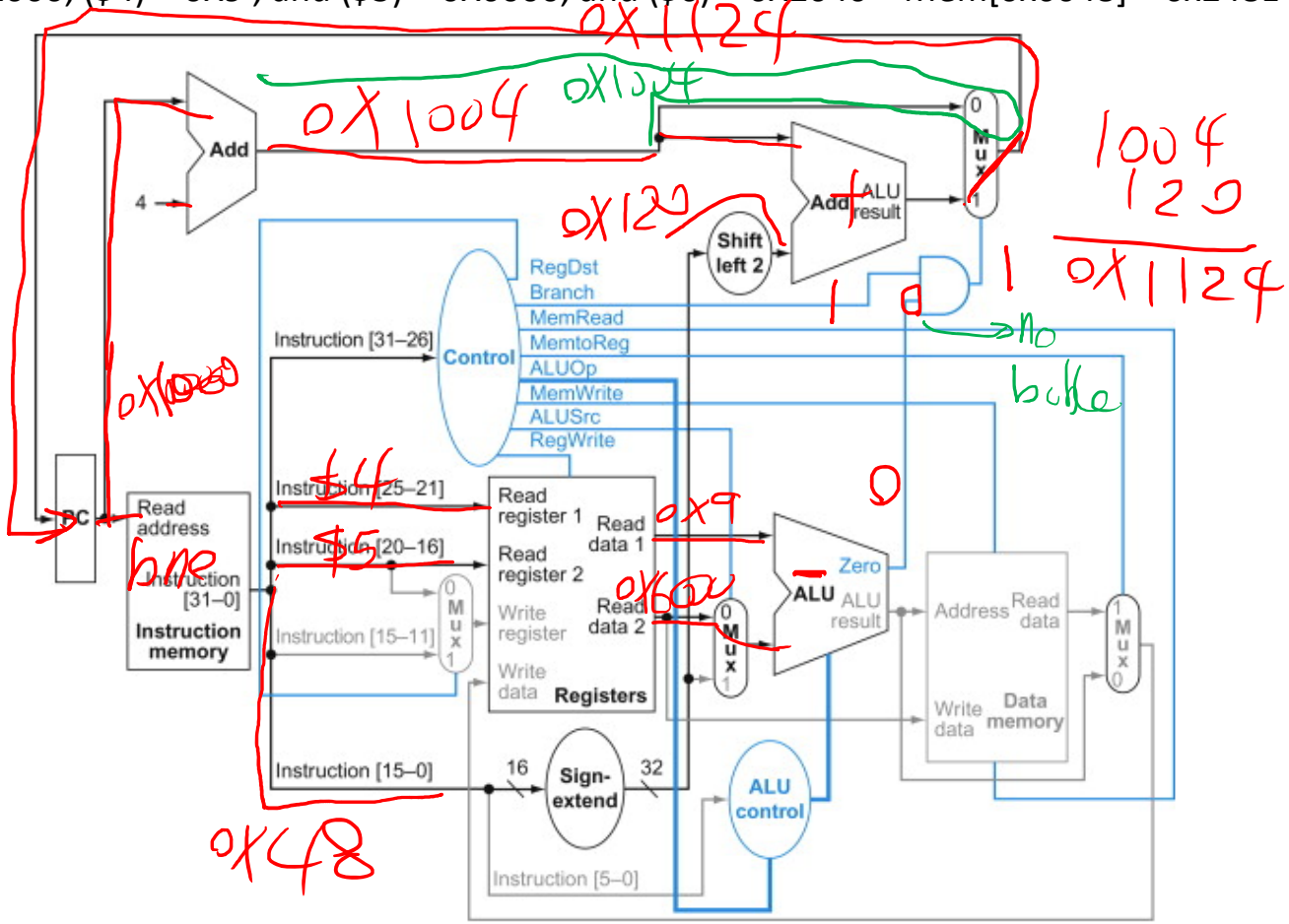
17)Highlight the active data path for: *bne $4, $5, 0x48*

Annotate the different segments of highlighted datapath with what they carry Assume the instruction is at memory location 0X1000, ($4) = 0X9 , and ($5) = 0X6000, and ($6) = 0X2040 Mem[0x6048] = 0x248E

After execution:

$4 =

$5=

$6=

PC=